CLAIMS

1. A semiconductor device comprising:

a logic portion;

a memory portion;

a detecting portion for detecting at least one of an operation frequency of the logic portion and an operation frequency of the memory portion;

a Vth control for supplying a Vth control signal to at least one of the logic portion and the memory portion depending on a detection result from the detecting portion; and

an antenna,

wherein each of the logic portion and the memory portion comprises at least one transistor;

wherein the at least one transistor has a first gate electrode which is input with a logic signal and a second gate electrode which is input with the Vth control signal, and

wherein at least the logic portion is provided with electric power from the antenna.

2. A semiconductor device comprising:

a logic portion;

a memory portion;

a detecting portion for detecting at least one of an operation frequency of the logic portion and an operation frequency of the memory portion;

a Vth control for supplying a Vth control signal to at least one of the logic portion and the memory portion depending on a detection result from the detecting portion; and

an antenna,

wherein each of the logic portion and the memory portion comprises at least one transistor,

wherein the at least one transistor has a first gate electrode which is input with a

logic signal, a second gate electrode which is input with the Vth control signal, and a semiconductor film,

wherein the semiconductor film is provided over the second gate electrode,

wherein the first gate electrode is provided over the semiconductor film, and

wherein at least the logic portion is provided with electric power from the antenna.

3. A semiconductor device according to any one of claims 1 and 2,

wherein the logic portion comprises more than one of a control circuit, an arithmetic circuit, an input/output circuit, a power source circuit, a clock generating circuit, a data demodulation/modulation circuit, and an interface circuit.

4. A semiconductor device according to any one of claims 1 and 2,

wherein the logic portion comprises a timing control, an instruction decoder, a register array, an address logic and buffer, a data bus interface, an ALU (Arithmetic Logic Unit), and an instruction register.

5. A semiconductor device according to any one of claims 1 and 2, wherein the memory portion comprises one or more of a DRAM, an SRAM, an FeRAM, a masked ROM, a fuse PROM, an anti-fuse PROM, EPROM, an EEPROM, and a flash memory.

6. A semiconductor device according to any one of claims 1 and 2, wherein the detecting portion is a program or a storage medium storing the program.

7. A semiconductor device according to any one of claims 1 or 2, wherein the at least one transistor is provided over a substrate.

8. A semiconductor device according to any one of claims 1 and 2, wherein the at least one transistor and the antenna are provided over a substrate.

9. A semiconductor device according to any one of claims 1 and 2, further comprising a first substrate and a second substrate,

wherein the at least one transistor is provided adjacent to the first substrate,

wherein the antenna is provided adjacent to the second substrate, and

wherein the first substrate and the second substrate are attached such that the at least one transistor and the antenna are electrically connected to each other.

10. A semiconductor device according to claim 7, wherein the substrate is one of a glass substrate and a flexible substrate.

11. A semiconductor device according to claim 8, wherein the substrate is one of a glass substrate and a flexible substrate.

12. A semiconductor device according to claim 9, wherein each of the first and second substrates is one of a glass substrate and a flexible substrate.